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情報通信技術

高冷却性能のマイクロチャンネル構造を形成した3D集積システム

TECHNOLOGY SHOWCASE

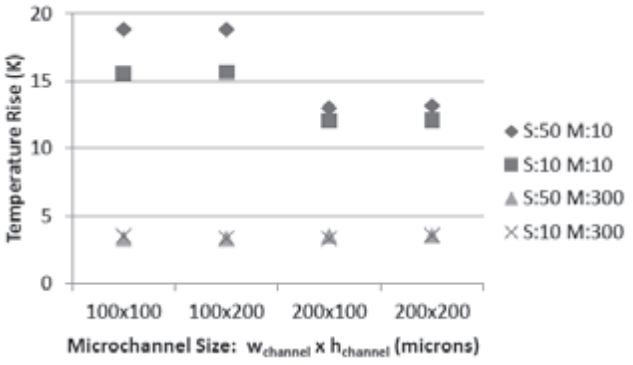
SATテクノロジー・ショーケース2014

■ はじめに

In order to increase circuit performance, the electronics industry has begun to vertically stack thinned circuits into three dimensional integrated circuits (3DICs). In 3DICs, heat generating devices are further away from the heatsink and power densities are higher than in traditional circuits. This results in a degraded thermal path which makes it more challenging to remove heat from the circuit.

Designing a high-performance, thermally-viable circuit using thinned wafers presents a significant challenge. Wafer thinning is necessary to achieve small, low aspect-ratio through-silicon vias (TSVs) to electrically connect between circuits in the vertical, however such thinning significantly decrease since the ability of the system to spread heat out from areas of high power dissipation. That is because the silicon wafer itself is a very good heat spreader, and without it small areas with high power dissipation can become large thermal problems.

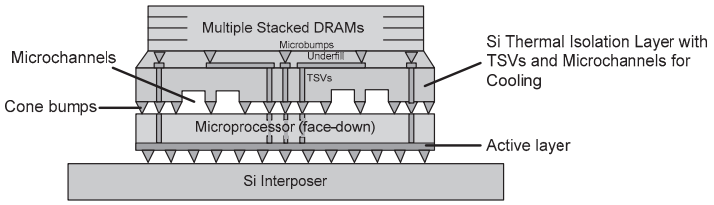
In memory-on-logic systems there is a significant concern that high-power sections of the processor will create large thermal gradients that cause logical failures in the stacked memory. Integrating microchannels for fluid-based cooling offers a way to remove heat directly from between the microprocessor and memory.



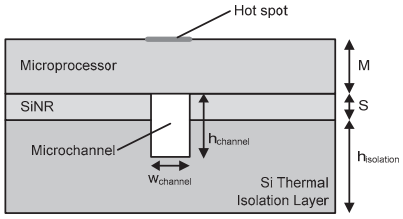
Maximum temperature rise at top of plane A-A' for various combinations of microprocessor height (M) and SiNR bonding layer thickness (S) in microns

■ 活動内容

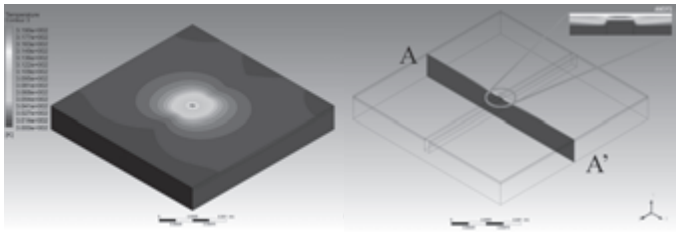
1. Development of a silicon thermal isolation layer that includes both TSVs for electrical connections and microchannels for cooling.
2. Development of conical bump technology to allow for high-reliability interconnections between wafers, even when planarity is compromised.
3. Investigation of the effect of wafer thickness, bonding layer thickness and microchannel sizing on the thermal performance of the system. We have found that at die thicknesses of 300 μm the hotspot temperature is fairly independent of design parameters. At 10 μm the microchannel width and SiNR bonding layer thickness plays a large role is determining maximum temperature.



Cross-section of target memory-on-logic system



Cross-section of ANSYS Model



Temperature profile calculated by ANSYS

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■キーワード:（1）3D 集積システム
（2）水冷
（3）マイクロチャンネル