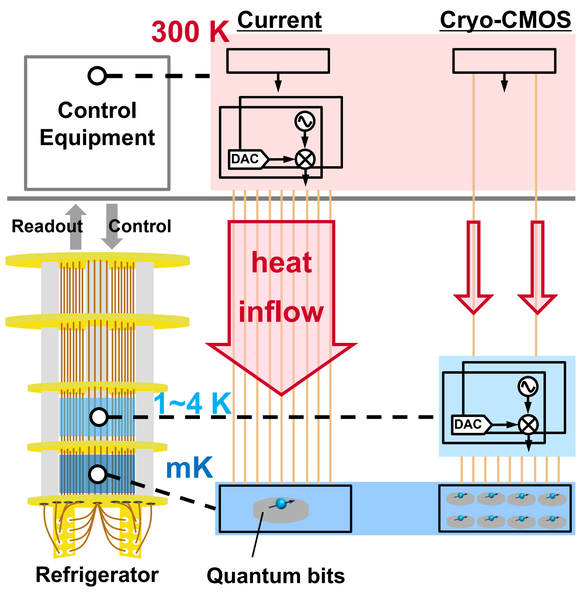
Characterization of Cryogenic MOSFETs for Qubit-Control Circuits

Introduction

- Cryo-CMOS is a key technology for realizing large-scale quantum computers by reducing the number of interconnects between room-temperature electronics and qubits.



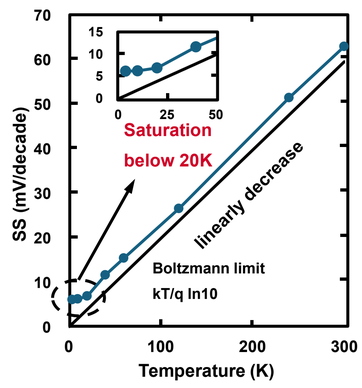
Cryogenic Operation of Si MOSFETs

- At cryogenic temperatures, various device parameters deviate from those predicted by conventional theory for room-temperature operation.
  - ➡ A physical understanding of cryogenic Si MOSFET characteristics is important.

Unique phenomena reported at CTs.

- Subthreshold-swing (SS) saturation
- Threshold-voltage shift
- Mobility enhancement
- 1/f-noise enhancement

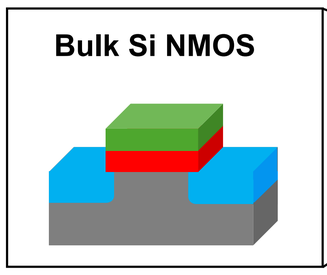
***SS-T* Characteristics for Long Gate Length**

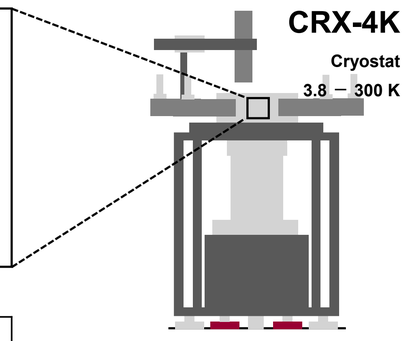


Purpose of This Work

- We aim to evaluate the gate-length dependence of SS at cryogenic temperatures.

Experimental Setup





Channel	NMOS
Gate Width	100 um
Gate Length	5, 10, 50, 100 um
Gate Stack	Poly-Si/SiO_2 (6 nm)
Orientation	(100)

Gate-Length Dependence of Subthreshold Swing at RT and 3.8 K

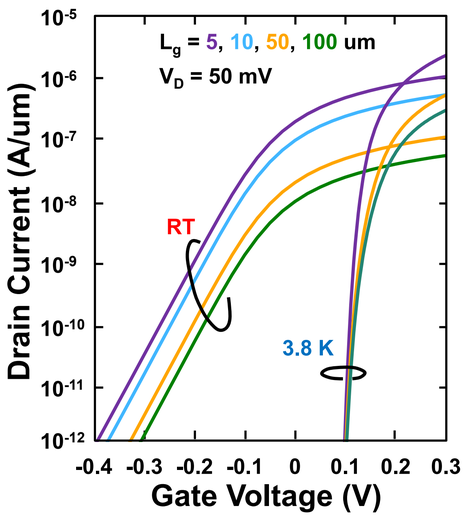
At room temperature (RT)

- Low-current region (10^{-12} ~ 10^{-10} A/um):
  - The SS does not depend on gate length.
    ⇔ The current is dominated by the diffusion component.
- High-current region (10^{-10} ~ 10^{-7} A/um):
  - The SS depends on gate length, and the shorter Lg results in the larger SS.
    ⇔ The current is dominated by the drift component.

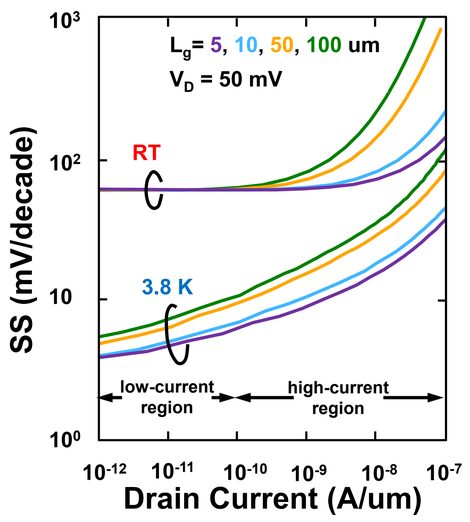
At 3.8 K (CT)

- Entire current range (10^{-12} ~ 10^{-7} A/um):
  - The SS depends on gate length, and the shorter Lg results in the larger SS.
    ➡ A similar trend to that in the high-current region at RT!

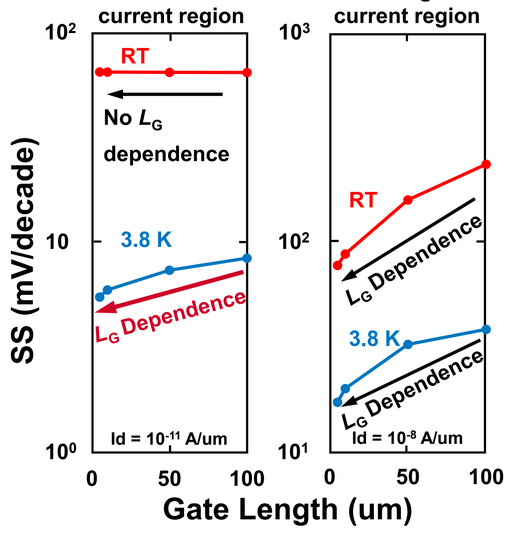
***I_D-V_G* Characteristics**



***SS-I_D* Characteristics**



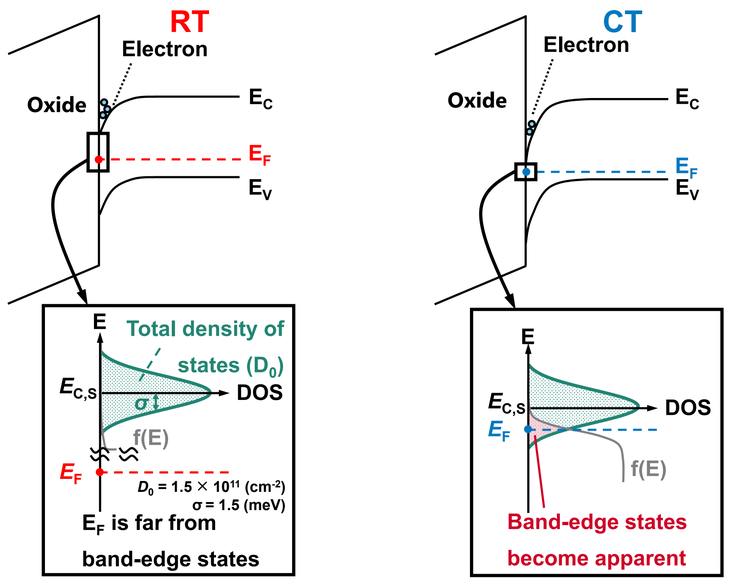
L_G* Dependence of *SS



Simulations for CT

- Fermi level approaches conduction band edge at LT.
- Band-edge states near the conduction band edge greatly affect cryogenic MOSFET operation.
- We introduced the Gaussian-type band-edge states in TCAD simulations at CT [1,2].

Band Diagram at Threshold Voltage Condition

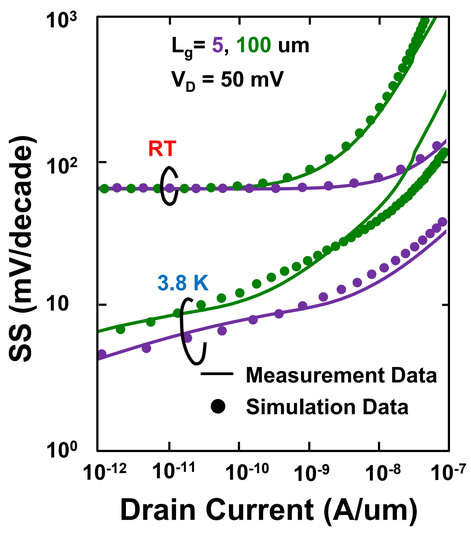


1) M. Kang et al., Jpn. J. Appl. Phys. 62, SC1062 (2023). 2) Y. Kobayashi et al., Jpn. J. Appl. Phys. 63, 094001 (2024).

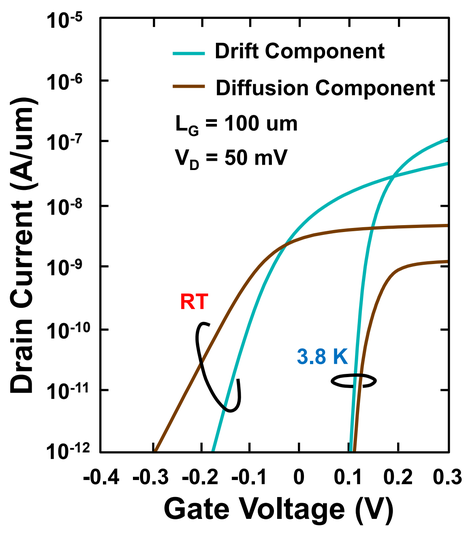
Origin of Unique Gate-Length Dependence of Cryogenic SS

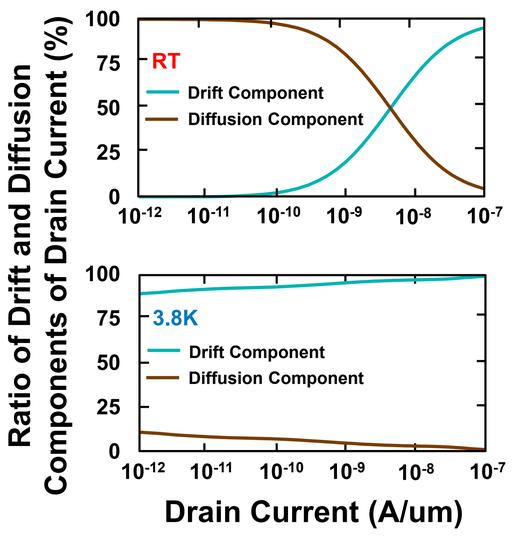
- Simulations using a band-edge states model reproduced the measured I_D–V_G and *SS*–I_D curves well.
- At RT, the dominant current component shifts from the diffusion to the drift as the drain current increases.
- At CT, the drift component dominates in entire current range.
  - ➡ The gate-length dependence of cryogenic SS originates from the drift current that stays dominant even in the low-current region.

***SS-I_D* Characteristics: Simulation and Measurement Data**



The Drift and Diffusion Components of Drain Current





- At CT, the gate-length dependence appears even in the low-current region, unlike under room-temperature operation.
- The gate-length dependence of cryogenic SS is caused by the drift current, which remains dominant even in the low-current region.

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